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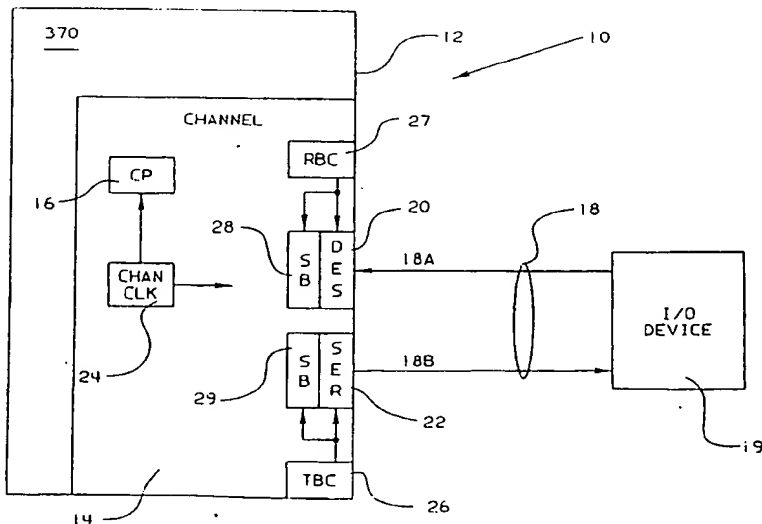
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(54) Data synchronizing buffer.

(57) Synchronizing buffer which synchronizes data link data with the channel clock (24) such that one character is transmitted onto the data link (18) for each channel clock. The synchronising buffer disclosed includes a first-in-first-out (FIFO) buffer which receives data characters from a data channel buffer, and outputs them onto the data link (18). When the

channel clock (24) is stopped, the synchronizing buffer circuit places idle characters on the data link with the proper disparity. When the channel clock (24) restarts, the circuit synchronises the sending of restarted data characters with the idle characters placed onto the link such that there is an intelligible string of characters on the data link at all times.

FIG. 1



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EUROPEAN SEARCH REPORT

Application Number

EP 90 11 7825

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	IBM TECHNICAL DISCLOSURE BULLETIN vol. 9, no. 10, March 1967, NEW YORK US pages 1334 - 1335 DALES AND MIZZI 'First - in, first - out buffer controls' * the whole document *	1,3,5,6, 9	H04L25/36 G06F5/06
A	EP-A-0 206 743 (TEXAS INSTRUMENTS INC.) * abstract; figures 2,4 *	1,3,5,6, 9	
A,P	IBM TECHNICAL DISCLOSURE BULLETIN vol. 32, no. 10A, March 1990, NEW YORK US pages 345 - 348 'Method of data synchronization on an asynchronously clocked interface' * figure 2 * * page 346, paragraph 2 * * page 347, paragraph 5 *	1,3-6,9	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H04L
G06F

The present search report has been drawn up for all claims

Place of search
THE HAGUE

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Examiner
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CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another
document of the same category
A : technological background
O : non-written disclosure
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or
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